TITLE **400G OSFP56 SR8 Transceiver**	**DOC No. RFD-20231115006-001**	
	REVISION：01	**AUTHORIZED BY：Andy Yang**
	DATE：2023.11.29	**CLASSIFICATION：CONFIDENTIAL**

1.Introduction

OSFP SR8 transceiver module is designed for use in 400 Gigabit Ethernet links over 70m OM3 or 100m OM4 fiber. The module has 8 independent electrical input/output channels operating at 53.125Gbps per channel. This transceiver consists of two transmitter/receiver units, with each operating on 850nm wavelength. The transmitter path of the module incorporates a PAM4 re-timer ASIC with two 4-channel modulator drivers and 8 modulated lasers. On the receiver path, it consists of 8 photodiodes and two 4-channel TIAs, along with the PAM4 re-timer. The electrical interface of the module is compliant with the 400GAUI-8 interface as defined by IEEE 802.3bs, and compliant with OSFP MSA

.2.Feature

- Supports 425Gbps
- Single 3.3V Power Supply
- Power Dissipation < 10W
- OSFP MSA Compliant
- 8x26.5625GBd (PAM4) Electrical Interface
- MPO-16 Connector APC
- Completely Independent 8 Channels to Support Break-out
- Case Temperature Range: 0°C to 70°C
- VCSEL Transmitter
- PIN and TIA Array on the Receiver Side
- I2C Interface with intergrated Digital Diagnostics Monitioring Safety
- Certification: TUV/UL/FDA
- 1x400GbE
- 2x200GbE
- 4x100GbE
- 8x50GbE
- Optical 50G PAM-4 per Lane

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3.PRODUCT DESCRIPTION

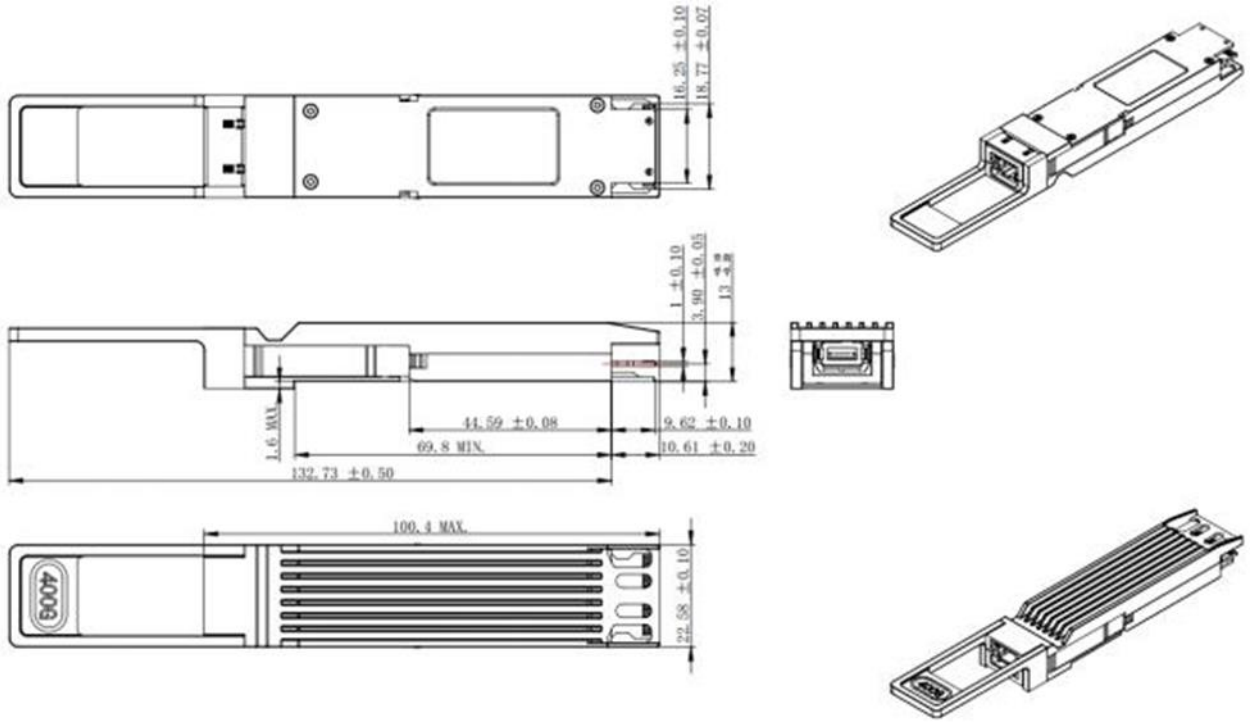
3.1PRODUCT NAME AND SERIES NUMBER(S)

400G OSFP56 SR8 Transceiver

Part Number	Data Rate	Wavelength (nm)	Distance	Power (dBm)	Sen. (dBm)	Connector	Temp.
P69008GQCA01-1	425G	850	70m(OM3) 100m(OM4)	-6.5~4	-6.5	MPO-16	C

3.2DIMENSIONS, MATERIALS, PLATINGS AND MARKING

The module is designed to meet the package outline defined in the OSFP56 specification. See the package outline for details.



Mechanical Package Outline (All dimensions in mm)

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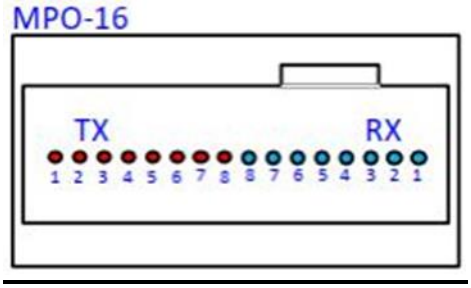
The optical interface port is a male MPO-16 connector as specified in TIA-604-18.



4.Product Specification

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	TS	-40	85	degC	
Power Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	5	85	%	

4.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	TOP	0		70	degC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Receiver Differential Data Output Load			100		Ohm	
Power Supply Noise				625	mVpp	1
Fiber Length (OM3)				70	m	
Fiber Length (OM4)				100	m	

Note

1: Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See recommended power supply filter.

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4.3 General Electrical Characteristics

Parameter	Test Point	Min	Typical	Max	Units
Power Consumption				10	W
Supply Current	Icc			3030	mA
AC Coupling Internal Capacitor		0.1			μF

4.4 Reference Points

Parameter	Test Point
TP1 and TP4	TP1 and TP4 are informative reference points that may be useful to implementers for testing components.
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3cm 138.7.1 are made at TP2.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3cm 138.7.2 are made at TP3.

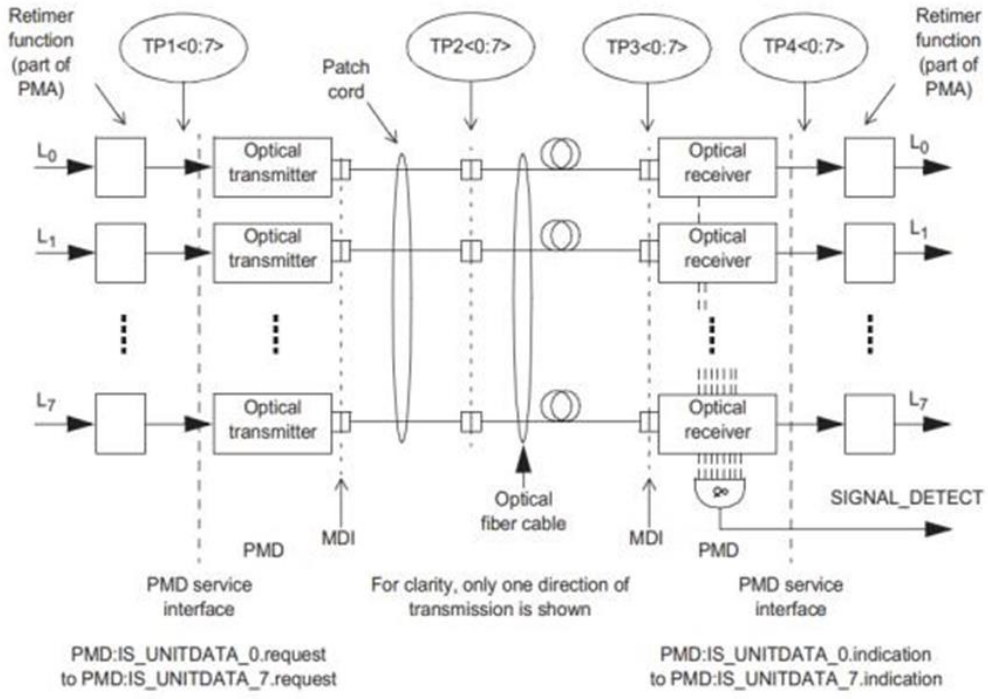

Figure 1: IEEE 802.3cm Block Diagram for 400GBASE-SR8 Transmit/Receive Paths

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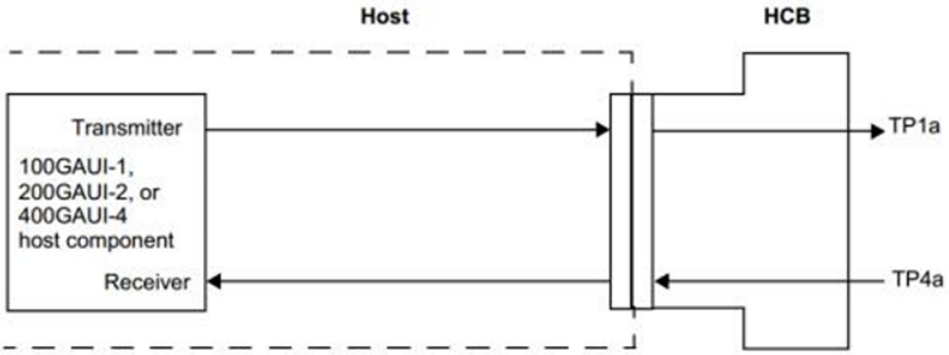

Figure 2: IEEE 802.3ck 400GAUI-4 compliance points TP1a, TP4a

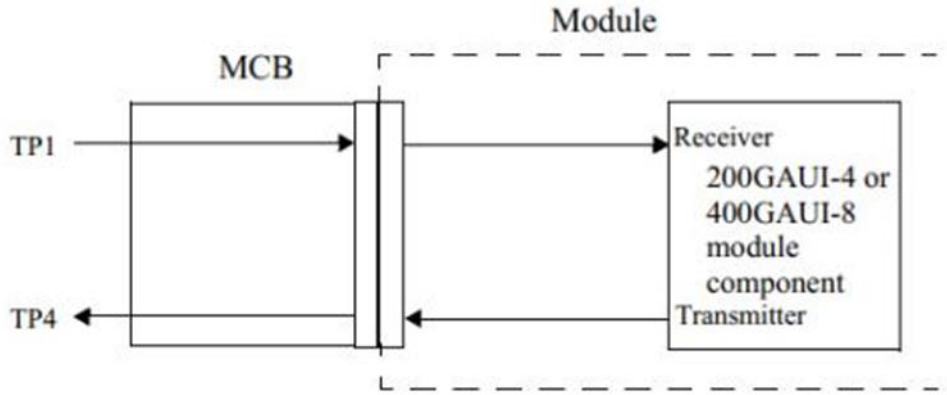

Figure 3: IEEE 802.3bs 400GAUI-8 C2M Compliance Points TP1, TP4

4.5 High Speed Electrical Input Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Signaling Rate, each Lane	TP1	26.5625+/- 100 ppm			GBd	
Differential peak-peak voltage tolerance	TP1a	900			mV	1
Differential Input Return Loss	TP1	Equation (83E-5)*8			dB	2
Common To Differential Mode Conversion Return Loss	TP1	Equation			dB	2

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		(83E-5)*8				
Differential Termination Mismatch	TP1			10	%	
Module Stressed Input Test	TP1a					3
Single-ended voltage	TP1a	-0.4		3.3	V	
DC common-mode voltage tolerance range	TP1	-350		2850	mV	4
Eye Width			0.22		UI	
Applied peak-peak sinusoidal jitter			Table 120E-6			5
Eye height			32		mV	

1: With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

2: Equation (83E-5) and Equation (83E-6) refer to IEEE 802.3-2018.

3: Meets BER specified in 120E.1.1 of IEEE 802.3-2018

4: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

5: Table 120E-6 refers to IEEE 802.3-2018.

4.6 High Speed Electrical Output Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Signaling Rate, each Lane(range)	TP4		26.5625 +/- 100 ppm		GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mV	
AC Common-Mode Output Voltage	TP4			17.5	mV	
Near-end ESMW (Eye Symmetry Mask Width)	TP4	0.265			UI	
Near-end Eye Height, Differential	TP4	70			mV	
Differential Output Return Loss	TP4	Equation			dB	1

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		(83E-2)*12				
Common to Differential Mode Conversion Return Loss	TP4	Equation (83E-3)*12				1
Differential termination mismatch	TP4			10	%	
Transition time	TP4	9.5			ps	
DC Common Mode Voltage	TP4	-350		2850	mV	2

Note

1: Equation (83E-2) and Equation (83E-3) refer to IEEE 802.3-2018.

2: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

4.7 High Speed Optical Transmitter Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Signaling speed, each lane	DR		26.5625± 100ppm		GBd	
Modulation format		PAM4				
Lane wavelength	λ	840		868	nm	
RMS Spectral Width	△λrms			0.6	nm	1
Extinction ratio, each lane	ER	3			dB	
Average launch power, each lane		-6,5		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each Lane	Poma	-4.5		3	dBm	2
Launch Power in OMAouter minus TDECQ	OMA-TDECQ	-5.9			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			4.5	dB	
TDECQ-10log10 (Ceq), each Lane	TDECQ-10log10 (Ceq)			4,5		3

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RIN12OMA	RIN12OMA			-128	dB/Hz	
Average launch power of OFF transmitter, each lane	Poff			-30	dBm	
Optical return loss tolerance	ORL			12	dB	
Encircled Flux	EF		≥86% at 19 μm			4
			≤30% at 4.5 μm			

Note

1: RMS spectral width is the standard deviation of the spectrum.

2: Even if the TDECQ < 1.4dB, the OMA (min) must exceed this value.

3: Ceq is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

4: If measured into type A1a.2 or type A1a.3, or A1a.4, 50um fiber, in accordance with IEC61280-1-4.

4.8 High Speed Optical Receiver Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Signaling speed, each lane	DR		26.5625± 100ppm		GBd	
Modulation Format		PAM4				
Lane wavelength λ	λ	840		868	nm	
Damage threshold		5			dBm	1
Average receiver power, each lane		-8.4		4	dBm	2
Receiver Power, each Lane (OMAouter)				3	dBm	
Stressed Receiver (OMAouter), each Lane				-3.4	dBm	3
LOS Assert	LOSA	-17			dBm	
LOS De-Assert	LOSD			-11	dBm	

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Receiver Sensitivity (OMAouter), each Lane			max (-6.5, SECQ-7.9)		dBm	4
Conditions of Stressed Receiver Sensitivity test						5
Stressed Eye Closure for PAM4 (SECQ), Lane under Test				4.5	dB	
SECQ-10log10 (Ceq)*23, Lane under Test				4.5	dB	6
OMA_{outer} of each Aggressor Lane*24			3		dBm	7
Receiver reflectance				-12	dB	

Note

1: The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

2: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

3: Measured with conformance test signal at TP3 (see 138.8.10) for the BER specified in 138.1.1.

4: Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5dB with BER<2.4x10-4 without FEC in PRBS 231-1.

5: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

6: Ceq is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

7: Only applies to 100GBASE-SR2 and 200GBASE-SR4 and 400GBASE-SR8.

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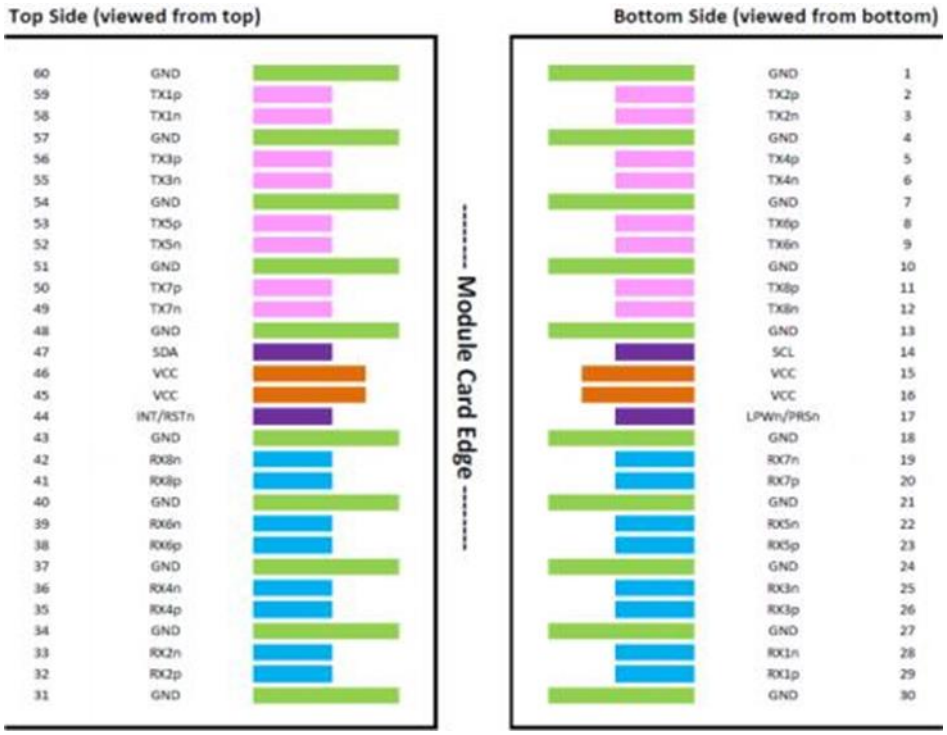
5.Pin Assignments



OSFP Pad Function Definition

Electrical Pin Definition(OSFP)

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2p	Transmitter Data Non-Inverted	3	
3	CML-I	Tx2n	Transmitter Data Inverted	3	
4		GND	Ground	1	1
5	CML-I	Tx4p	Transmitter Data Non-Inverted	3	
6	CML-I	Tx4n	Transmitter Data Inverted	3	
7		GND	Ground	1	1
8	CML-I	Tx6p	Transmitter Data Non-Inverted	3	

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9	**CML-I**	**Tx6n**	**Transmitter Data Inverted**	**3**	
10		**GND**	**Ground**	**1**	**1**
11	**CML-I**	**Tx8p**	**Transmitter Data Non-Inverted**	**3**	
12	**CML-I**	**Tx8n**	**Transmitter Data Inverted**	**3**	
13		**GND**	**Ground**	**1**	**1**
14	**LVCMOS-I/O**	**SCL**	**2-wire Serial interface clock**	**3**	**2**
15		**VCC**	**+3.3V Power**	**2**	
16		**VCC**	**+3.3V Power**	**2**	
17	**Multi-Level**	**LPWn/PRSn**	**Low-Power Mode/Module**	**3**	
18		**GND**	**Ground**	**1**	**1**
19	**CML-O**	**Rx7n**	**Receiver Data Inverted**	**3**	
20	**CML-O**	**Rx7p**	**Receiver Data Non-Inverted**	**3**	
21		**GND**	**Ground**	**1**	**1**
22	**CML-O**	**Rx5n**	**Receiver Data Inverted**	**3**	
23	**CML-O**	**Rx5p**	**Receiver Data Non-Inverted**	**3**	
24		**GND**	**Ground**	**1**	**1**
25	**CML-O**	**Rx3n**	**Receiver Data Inverted**	**3**	
26	**CML-O**	**Rx3p**	**Receiver Data Non-Inverted**	**3**	
27		**GND**	**Ground**	**1**	**1**
28	**CML-O**	**Rx1n**	**Receiver Data Inverted**	**3**	
29	**CML-O**	**Rx1p**	**Receiver Data Non-Inverted**	**3**	
30		**GND**	**Ground**	**1**	**1**
31		**GND**	**Ground**	**1**	**1**
32	**CML-O**	**Rx2p**	**Receiver Data Non-Inverted**	**3**	
33	**CML-O**	**Rx2n**	**Receiver Data Inverted**	**3**	
34		**GND**	**Ground**	**1**	**1**
35	**CML-O**	**Rx4p**	**Receiver Data Non-Inverted**	**3**	
36	**CML-O**	**Rx4n**	**Receiver Data Inverted**	**3**	
37		**GND**	**Ground**	**1**	**1**

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38	**CML-O**	**Rx6p**	**Receiver Data Non-Inverted**	**3**	
39	**CML-O**	**Rx6n**	**Receiver Data Inverted**	**3**	
40		**GND**	**Ground**	**1**	**1**
41	**CML-O**	**Rx8p**	**Receiver Data Non-Inverted**	**3**	
42	**CML-O Rx8n**	**Rx8n**	**Receiver Data Inverted**	**3**	
43		**GND**	**Ground**	**1**	**1**
44	**Multi-Level**	**INT/RSTn**	**Module input/Module Reset**	**3**	
45		**VCC**	**+3.3V Power**	**2**	
46		**VCC**	**+3.3V Power**	**2**	
47	**LVCMOS-I/O**	**SCL**	**2-wire Serial interface Data**	**3**	**2**
48		**GND**	**Ground**	**1**	**1**
49	**CML-I**	**Tx7n**	**Transmitter Data Inverted**	**3**	
50	**CML-I**	**Tx7p**	**Transmitter Data Non-Inverted**	**3**	
51		**GND**	**Ground**	**1**	**1**
52	**CML-I**	**Tx5n**	**Transmitter Data Inverted**	**3**	
53	**CML-I**	**Tx5p**	**Transmitter Data Non-Inverted**	**3**	
54		**GND**	**Ground**	**1**	**1**
55	**CML-I**	**Tx3n**	**Transmitter Data Inverted**	**3**	
56	**CML-I**	**Tx3p**	**Transmitter Data Non-Inverted**	**3**	
57		**GND**	**Ground**	**1**	**1**
58	**CML-I**	**Tx1n**	**Transmitter Data Inverted**	**3**	
59	**CML-I**	**Tx1p**	**Transmitter Data Non-Inverted**	**3**	
60		**GND**	**Ground**	**1**	**1**

Note

1: OSFP uses common ground (GND) for all signals and supply (power). All are common module voltages are referenced to this potential unless otherwise noted.

2: Open-Drain with pull up resistor on Host.

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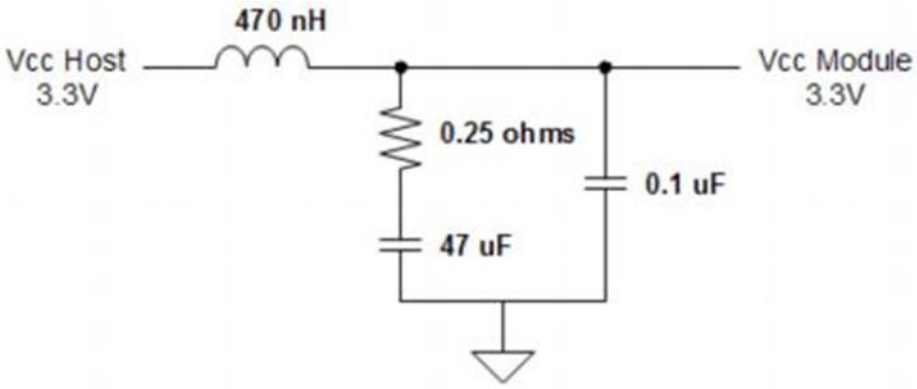
Recommended Power Supply Filter

For safety and protection of the host system, the power to each OSFP module may be protected by an electronic circuit breaker on the host board which is enabled with the H_PRSn signal such that power is only enabled when the module is fully engaged into the OSFP connector.



6. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2023/11/29	Andy Yang	Mike Sun